What is Claimed is:

1. A memory device, comprising:

a plurality of data I/O buffers connected one by one to a plurality of I/O ports;

a switch array comprising a plurality of switches for connecting the plurality of data I/O buffers to a plurality of sense amplifier arrays; and

a switch controller for receiving external control signals to control activation of each data I/O buffer and on/off operations of the plurality of switches.

2. A memory device, comprising:

a data I/O buffer connected to an I/O port for inputting/outputting a plurality of data bits;

a switch array comprising a plurality of switches for transmitting data between the data I/O buffer and a sense amplifier array for processing data by a predetermined number of data bits; and

a switch controller for receiving external control signals to control on/off operations of the plurality of switches.

3. A memory device, comprising:

a plurality of data I/O buffers connected one by one to a plurality of I/O ports for inputting/outputting a plurality of data bits;

a switch array comprising a plurality of switches for connecting the data I/O buffers and a sense amplifier array for processing data by a predetermined number of data bits; and

a switch controller for receiving external control signals to control activation of the plurality of data I/O data buffers and on/off operations of the plurality of switches.

4. The memory device according to claim 3, wherein the switch controller receives one of the external control signals via one of the I/O ports.

5. A memory device, comprising:

a switch array comprising a plurality of first switches for connecting a lower byte region of a data I/O buffer to a lower byte region of a sense amplifier array, a plurality of second switches for connecting a lower byte region of a data I/O buffer to an upper byte region of the sense amplifier array, and a plurality of third switches for connecting an upper byte region of a data I/O buffer to the upper byte region of the sense amplifier array; and

a switch controller for receiving external control signals to control activation of the data I/O buffer and on/off operations of the first through the third switches.

6. The memory device according to claim 5, wherein the switch controller turns on the first switch and activates the lower byte region of the data I/O buffer connected to an I/O port when a lower signal included in the external control signal is activated, and turns on the third switch and activates the upper byte region of the data I/O buffer connected to an I/O port when an upper byte signal included in the external control signal is activated.

7. The memory device according to claim 5, wherein the lower byte

region of the data I/O buffer is connected to an I/O port, the upper byte region of the data I/O buffer is not connected to an I/O port, and an external control signal included in the external signals is provided through a terminal pin connected to the upper byte region of the data I/O buffer.

8. The memory device according to claim 7, wherein the switch controller activates the first switches when a control signal inputted through the terminal pin is "0", and the second switches when a control signal inputted through the terminal pin is "1".

9. The memory device according to claim 5, wherein the switch controller inactivates the upper byte region of the data I/O buffer and activates the second switches if a signal inputted through a terminal pin connected to the upper byte region is "1", and activates the first switches if a signal inputted through the terminal pin is "0" when a byte signal included in the external control signals is activated, and

the switch controller turns on the first switches and then activates a lower byte region of the data I/O buffer if a lower byte signal included in the external control signals is activated, and turns on the third switches and then activates an upper region of the data I/O buffer if an upper byte signal included in the external control signal is activated when the byte signal is inactivated.

10. The memory device according to claim 1, wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

11. The memory device according to claim 2, wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

12. The memory device according to claim 3, wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

13. The memory device according to claim 5, wherein the memory device is a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

14. A memory device, comprising:

buffer means for receiving and outputting a plurality of data bits in response to a buffer control signal, the buffer means coupled to a plurality of data I/O pin means for providing electrical connections to external circuits;

sense means for sensing and amplifying a plurality of data bits;

switch means for connecting the buffer means to the sense means in response to a switch control signal; and

control means for receiving external control signals, at least one of which is received via one or more of the plurality of the data I/O pins, and controlling the buffer means by providing the buffer control signal and controlling the switch means by providing the switch control signal.

15. A method for operating an electronic memory device that processes data by two bytes having a data buffer comprising an upper byte portion and a lower byte portion to enable the electronic memory device to operate with a system bus that processes data by one byte, comprising:

receiving an address bit on an input for the upper byte portion of the data buffer; and

using the address bit received on the input for the upper byte portion of the data buffer to control the output and input of data from/to the system bus.

16. A method for storing data provided by a system that processes data by one byte in an electronic memory device that stores data by two bytes associated with an address in the form of an upper byte portion and a lower byte portion, comprising the steps:

receiving a data byte and a one-byte address for the data byte from the system, the one-byte address having a least significant bit, wherein the least significant bit is received as an input to a upper byte portion of a data input/output; and

storing the received data byte to either the upper byte portion or the lower byte portion associated with the address in response to the least significant bit.

18. A memory device that processes data by two bytes comprising a lower byte and an upper byte that is capable of operating with a system that processes data by one byte, comprising:

a plurality of data pads configured to connect to the system;

a data input/output buffer coupled to the plurality of data pads and comprising a lower byte portion and an upper byte portion;

a circuit that stores data of the lower byte portion of the data input/output buffer to either an upper byte portion or a lower byte portion of data storing portion depending upon an external signal received on a data pad coupled to the upper byte portion of the data input/output buffer.

19. A system having an address bus capable of transmitting a data storage address, the address having a least significant bit, comprising:

a memory device coupled to the address bus, the memory device comprising:

a plurality of data I/O buffers comprising an upper byte region and a lower byte region connected one by one to a plurality of I/O ports;

a switch array comprising a plurality of switches for connecting the plurality of data I/O buffers to a plurality of sense amplifier arrays; and

a switch controller for receiving external control signals to control activation of each data I/O buffer and on/off operations of the plurality of switches,

wherein a portion of the address bus transmitting the least significant bit is coupled to one of the plurality of I/O ports connected to the upper byte region of the data I/O buffers.